

USSN 09/865,504  
Art Unit 2634  
Amdt dated Sep 6, 2005  
Reply to Office action of June 6, 2005

### Amendments to the Specification

Please amend paragraph [0055] as follows:

-- [0055] The first PLL 1 is referred to as an acquisition PLL and has a low pass filter 11 with a relatively high cut-off frequency. For example, 300KHz, so that the acquisition PLL tracks all changes in the input signal, including error components. The output [[3]] of the first PLL 1 is connected to the input of a second PLL 2, forming an output PLL and generating an output signal [[4]]. --

Please amend paragraph [0069] as follows:

--[0069] Figure 8 shows a similar circuit connected to the output PLL2. Several acquisition PLLs are connected to output PLL2 through an a functional block 5 in the form of an equation operator, in this case an adder, that sums the reference inputs (with or without weighting factors) to yield some the average frequency of several inputs.--

Please amend paragraph [0070] as follows:

-- [0070] Figure 9 shows a more generalized model for three acquisition PLLs and one output PLL 2, where the output PLL receives some mathematical combination of the outputs of the acquisition PLLs1 through operational the functional block 5 in the form of an equation operator. The equation may encompass non-linear equations, such as the MUX 3, but and also time dependent equations, normal linear equations etc. Of course the number of acquisition and output PLLs may be changed.

Please amend paragraph [0071] as follows:

[0071] Figure 10 shows a plurality of acquisition PLLs 1 connected through operational functional block 5 in the form of an equation operator to output PLL 1. The acquisition PLLs 1 are connected through Muxes 6 to three inputs in1, in 2, in 3 and crystal oscillator 7. This embodiment allows the quality of the circuits to be tested. --